[0024] It is then possible to apply an intermediate insulating layer **17** in the edge region **12** of the capacitance-increasing field plate structure **15** simultaneously with the application of an intermediate insulating layer **27** in the cell field **9** and with the opening of through-plated holes **16** to the field plate structure **15** in the intermediate insulating layer **17**. Electrically conductive bond contact areas **13** are then applied in the edge region **12**, forming a bond with the capacitance-increasing field plate structure **15**. It is then possible to finish the semiconductor device **1** by, for example, dividing the semiconductor wafer into individual semiconductor chips and mounting it on a corresponding flat conductor frame. External contacts on the flat conductor frame are then connected via bond connections, for example, to the bond contact areas on the upper side **7** of the semiconductor chip. It is then possible to pour the semiconductor chip with the bond connections into a plastic package molding compound from which the external contacts project.

[0025] In one embodiment of the process the capacitance-increasing field plate **15** is positioned beneath a gate bond contact area **13** and set to gate potential by a contact via **16** through an intermediate insulating layer **17**. Instead of positioning the field plate structure **15** beneath a gate bond contact area **13** it is also possible to position such a field plate structure **15** beneath a source bond contact area **14** as illustrated in one of the following figures. In such cases the source bond contact area is then set to source potential via contact vias **16** through an intermediate insulating layer **17**. In one embodiment illustrated in FIG. **1**, the capacitance-increasing field plate **15** is electrically connected to near-edge trench gate electrodes of the cell field **9** and to a gate bond contact area **13**. This can be achieved by using the appropriate mask layouts.

[0026] In the embodiment illustrated in FIG. **1**, charge compensation zones **22** provided with a width b_1, b_2 and b_3 which decreases toward the edge region **12** at a constant stepwidth P are applied towards the edge region of the semiconductor body **12**. The advantages of a process of this type have already been described above and will not therefore be repeated here. In the transition region **30** towards the edge region **12**, instead of a decreasing width b the charge compensation zones **22** may be provided with a decreasing depth t at a constant stepwidth P, as illustrated in one of the following figures.

[0027] The application of an electrically conductive, capacitance-increasing field plate structure **15** to the field plate oxide layer **18** can be carried out simultaneously with the application of gate electrode material **28** in the cell field **9** by using the depositing and structuring of a highly doped polysilicon. The application of an intermediate insulating layer **17** in the edge region **12** of the capacitance-increasing field plate structure **15** can also be carried out simultaneously with the application of an intermediate insulating layer **27** in the cell region **9** by using the depositing and structuring of silicon oxide or silicon nitride.

[0028] Through-plated holes **16** to the field plate structure **15** in the intermediate insulating layer **17** can be opened by using etching—in one embodiment dry etching or plasma etching. The application of electrically conductive bond contact areas **13** in the edge region **12**, thereby forming a bond with the capacitance-increasing field plate structure **15**, can also be carried out by using the depositing and structuring of a metal layer.

[0029] FIG. **2** illustrates a schematic cross-section through a semiconductor device **2** as disclosed in a further embodiment. Components with functions identical to those illustrated in FIG. **1** are indicated by using the same reference numerals and are not described in greater detail here.

[0030] The edge region **12**/**12'** need not necessarily coincide with the lateral edge termination of the semiconductor device to ensure the electrical blockability between the edge **29** illustrated in FIG. **1** and the active area of the semiconductor device. In other embodiments, the edge region **12**/**12'** can also be a region inside the active area of the semiconductor device and/or between the active area of the semiconductor device and the lateral edge termination of the semiconductor device. The edge region **12'** illustrated in FIG. **2** is characterised in that in the case of blocking the space charge zone extends considerably closer to the device surface than in the active area with the compensation zones, thus considerably increasing the vertical space charge capacity in the region of the edge regions **12'**.

[0031] In one embodiment, a capacitance-increasing field plate structure **15** is provided in an edge region **12'**. In the view illustrated in FIG. **2**, the edge area **12'** is positioned in the centre of the figure at a distance from an electrical edge termination, while parts of the central cell field **9** are illustrated on either side. Between them are once again transition regions **30** in which the equipotential lines **25** and **31** are drawn up towards the upper side **7** of the semiconductor body **6** with relatively moderate radii of curvature. In this arrangement an n^+-conducting, near-surface zone **21** ensures that both the potential line **25** at maximum field strength and the potential line **31** run in the field plate oxide layer **18** at all times, thereby making it possible to increase the capacitance again above that of the example illustrated in FIG. **1** at identical boundary and initial conditions by 25% to 1.25 pF if, as illustrated in FIG. **1**, for example, the capacitance-increasing field plate structure **15** is positioned beneath a gate bond contact area in the edge region **12**.

[0032] In one embodiment illustrated in FIG. **2**, however, the field plate structure **15** is in contact not with a gate bond contact area, but with a source bond contact area **14**. This metal source bond contact area **14** is electrically connected to the field plate **15** by contact vias **16**. In this arrangement the field plate structure **15** extends to the upper side **7** of the semiconductor body **8** over both the transition regions **30** and the edge region **12**. In the cell region **9** the source bond contact area **14** turns into the source electrode and the source structure **11**.

[0033] In terms of the width of the charge compensation zones **22**, the transition regions **30** in FIG. **2** are designed in exactly the same manner as the transition zone **30** in FIG. **1** and will not therefore be described again at this point. In the production process it is, however, important to note that prior to the application of the field oxide layer **18** in the edge region **12** a highly doped, n^+-conducting zone **21** is inserted into the upper side **7** of the semiconductor body **6** in the edge region **12** in order to achieve the advantages set out above, namely the shifting of the equipotential lines from the semiconductor body **6** to the insulator of the field plate oxide layer **18**. With the structure illustrated in FIG. **2** it is possible to achieve an increase in source-drain capacitance C_{SD} which is only slightly dependent on voltage.

[0034] FIG. **3** illustrates a schematic cross-section through an alternative embodiment of the semiconductor device **2** illustrated in FIG. **2**. Components with functions identical to those illustrated in FIG. **2** are indicated by using the same reference numerals and not described in greater detail. In this